CDB4361

# Evaluation Board for CS4361

## Features

- Demonstrates recommended layout and grounding arrangements
- CS8416 receives S/PDIF, & EIAJ-340-compatible digital audio
- Header for External PCM Audio
- Requires only a digital signal source and power supplies for a complete digital-to-analog converter system

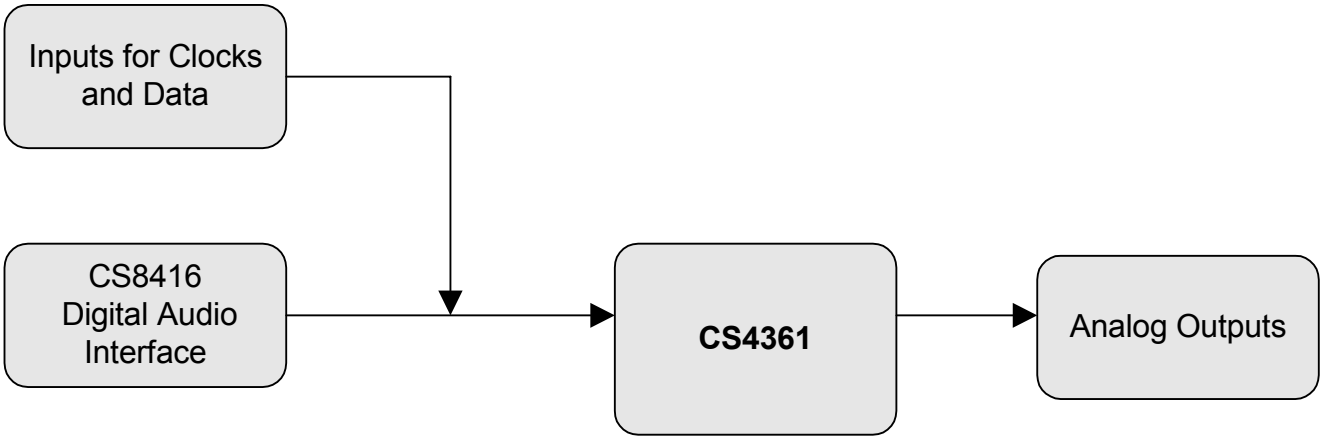
## Description

The CDB4361 evaluation board is an excellent means for quickly evaluating the CS4361 24-bit, 20-pin, 6-channel D/A converter. Evaluation requires an analog signal analyzer, a digital signal source, and a power supply. Analog line-level outputs are provided via RCA phono jacks.

The CS8416 digital audio receiver IC provides the system timing necessary to operate the digital-to-analog converter and will accept S/PDIF, and EIAJ-340-compatible audio data. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

**ORDERING INFORMATION**

| | |
|---|---|
| CDB4361 | Evaluation Board |



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## CDB4361 SYSTEM OVERVIEW

The CDB4361 evaluation board is an excellent means of quickly evaluating the CS4361. The CS8416 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply external PCM clocks and data through a PCB header for system development.

The CDB4361 schematic has been partitioned into six schematics shown in Figures 41 through 46. Each partitioned schematic is represented in the system diagram shown in Figure 40. Notice that the system diagram also includes the interconnections between the partitioned schematics.

## 1. CS4361 DIGITAL-to-ANALOG CONVERTER

A description of the CS4361 is included in the CS4361 datasheet.

## 2. CS8416 DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8416 Digital Audio Receiver, Figure 42. The outputs of the CS8416 include a serial bit clock, serial data, left-right clock, and a 128/256 Fs master clock. The CS8416 data format is selected using switch S3. The operation of the CS8416 and a discussion of the digital audio interface is included in the CS8416 datasheet.

The evaluation board has been designed such that the input can be either optical or coaxial, see Figure 42. However, both inputs cannot be driven simultaneously.

The bottom switch of S3 sets the output MCLK to LRCK ratio of the CS8416. This switch should be set to 256 (closed) for inputs Fs≤96 kHz and 128 (open) for Fs≥64 kHz. The 8416 must be manually reset using RESET (S1) when this switch is changed.

## 3. INPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via the header J37. Header J37 allows the evaluation board to accept externally generated PCM clocks and data. The schematic for the clock/data input is shown in Figure 43. The top switch of S3 selects the source as either CS8416 (open) or header J37 (closed).

Please see the CS4361 datasheet for more information.

## 4. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by two binding posts (GND and +5 V), see Figure 46. VL and VA can be jumpered separately to either the on board +3.3 V regulator or the +5 V binding post.

**WARNING:** Refer to the CS4361 datasheet for maximum allowable voltages levels. Operation outside of this range can cause permanent damage to the device.

## 5. GROUNDING AND POWER SUPPLY DECOUPLING

As with any high-performance converter, the CS4361 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 41 details the connections to the CS4361 and Figures 47, 48, and 49 show the component placement and top and bottom layout. The decoupling capacitors are located as close to the CS4361 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

## 6. ANALOG OUTPUT FILTERING

The analog output on the CDB4361 has been designed according to the CS4361 datasheet. This output circuit includes an AC coupling cap and a single pole R and C. An additional load resistance may be added by shunting J23, J24, J38, J39, J42, and J43 to test the CS4361's load-driving capability. See Figure 44 on page 20 for more details.

## 7. OPTIONAL MUTE CIRCUITRY

The CDB4361 contains the optional, recommended mute circuitry for the CS4361. This circuitry is designed to minimize the potential for clicks and pops. In order for this circuitry to operate properly, a negative supply is required. This supply is provided by U18. See Figure 45 on page 21 for more details.

| CONNECTOR | INPUT/OUTPUT | SIGNAL PRESENT |
|---|---|---|
| +5 V | Input | + 5 V power |
| GND | Input | Ground connection from power supply |
| S/PDIF INPUT - J1 | Input | Digital audio interface input via coax |
| S/PDIF INPUT - OPT1 | Input | Digital audio interface input via optical |
| PCM INPUT - J37 | Input | Input for master, serial, left/right clocks and serial data |
| AOUT1 - 6 | Output | RCA line level analog outputs |

**Table 1. System Connections**

| JUMPER / SWITCH | PURPOSE | POSITION | FUNCTION SELECTED |
|---|---|---|---|
| J46 | Selects source of voltage for the CS4361 VA supply | +3.3 V<br>*+5 V | Voltage source is a +3.3 V regulator<br>Voltage source is +5 V binding post |
| J17 | Provides contact points to measure VA current | - | Measure voltage across these nodes and divide result by 10 to get current in amps |
| J45 | Selects source of voltage for the CS4361 VL supply | +3.3 V<br>*+5 V | Voltage source is a +3.3 V regulator<br>Voltage source is +5 V binding post |
| J20 | Provides contact points to measure VL current | - | Measure voltage across these nodes and divide result by 10 to get current in Amps |
| J52 | CS4361 Mode Select | *I2S<br>LJ<br>RJ16<br>RJ24 | Sets the mode of the CS4361 by placing a shunt across the desired setting |
| J63 | Global Mute Enable | *shunted<br>open | Connects the CS4361 MUTEC pin to the mute circuitry<br>Disconnect for VA power-down current measurements |
| J53, J54<br>J55, J56<br>J57, J58 | Mute Enable | *shunted<br>open | When shunted, the mute circuit is active<br>When open, the mute circuit is inactive |
| J24, J23<br>J39, J38<br>J43, J42 | AC Load | shunted<br>*open | When shunted, a 3 kΩ AC load is added to the output<br>Leave open for normal operation |
| S1 | Resets CS4361 and CS8416 | | The CS8416 must be reset if switch S2 is changed |
| S2 | SDIN Control | *All closed<br>All open | Connects SDIN1 to SDIN2 and SDIN3<br>SDIN1, 2, and 3 are discrete |

| JUMPER / SWITCH | PURPOSE | POSITION | FUNCTION SELECTED |
|---|---|---|---|
| S3 | Sets clock source | 1 (top) EXT/8416 | Sets clock source for CS4361 (*open = CS8416, closed = J37) |
| | CS8416 Mode 0 | 2 RX_SF0 | Sets CS8416 serial data format (SF1, SF0) 00 = LJ24 *01 = I2S 10 = RJ24 |
| | CS8416 Mode 1 | 3 RX_SF1 | |
| | Sets MCLK ratio of CS8416 | 4 (bottom) | Selects 128x (open) or 256x (*closed) MCLK/LRCK ratio output for CS8416 |
| *Default Factory Settings | | | |

**Table 2. CDB4361 Jumper Settings**

# 8. PERFORMANCE PLOTS

The plots in the following section were acheived using an Audio Precision System 2700 and a randomly chosen production CDB4361. In some cases the performance may be limited by the CDB4361. All measurements were taken at room temp using the standard AP filter options (20 Hz to 22 kHz) with default board settings and nominal datasheet voltages applied unless otherwise noted.

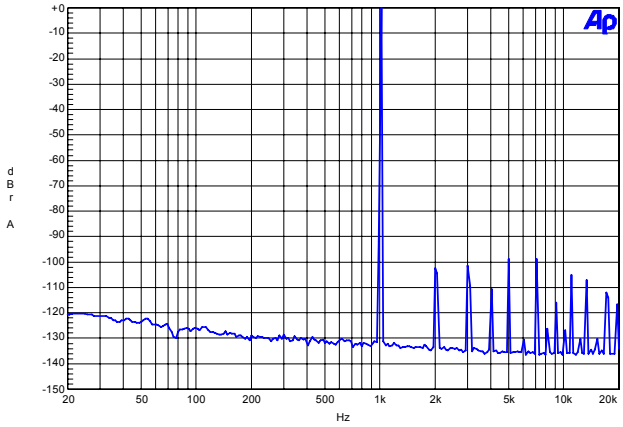



**Figure 1. FFT (48 kHz, 0 dB)**

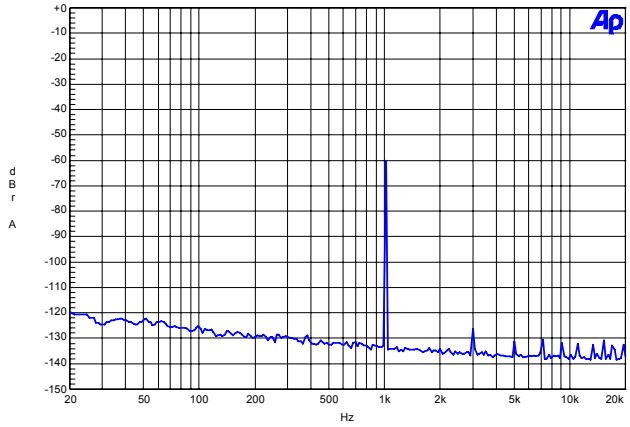



**Figure 2. FFT (48 kHz, -60 dB)**

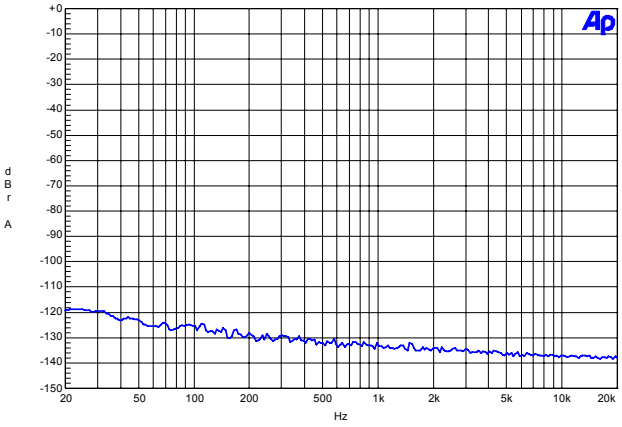



**Figure 3. FFT (48 kHz, No Input)**

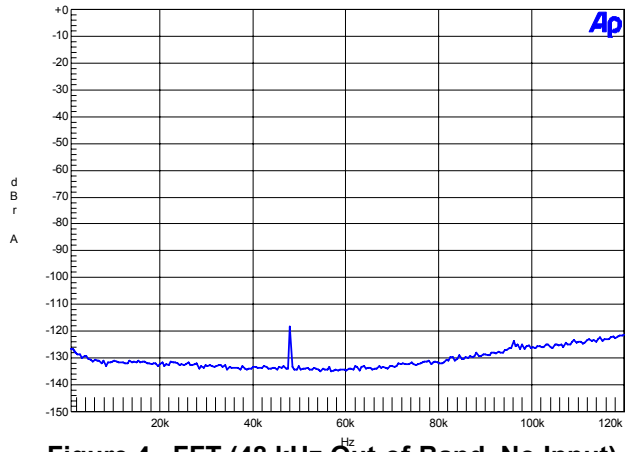



**Figure 4. FFT (48 kHz Out-of-Band, No Input)**

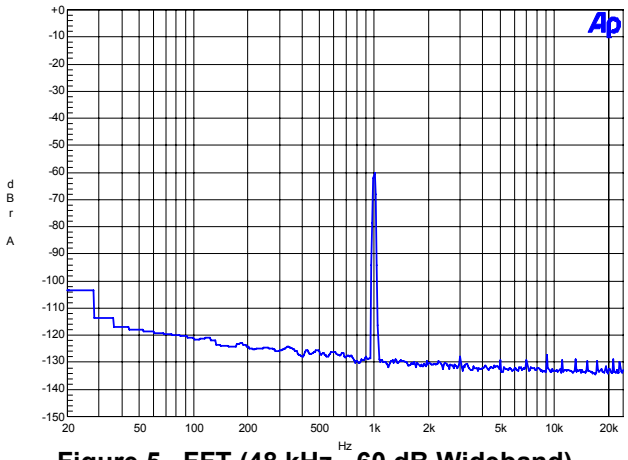



**Figure 5. FFT (48 kHz, -60 dB Wideband)**

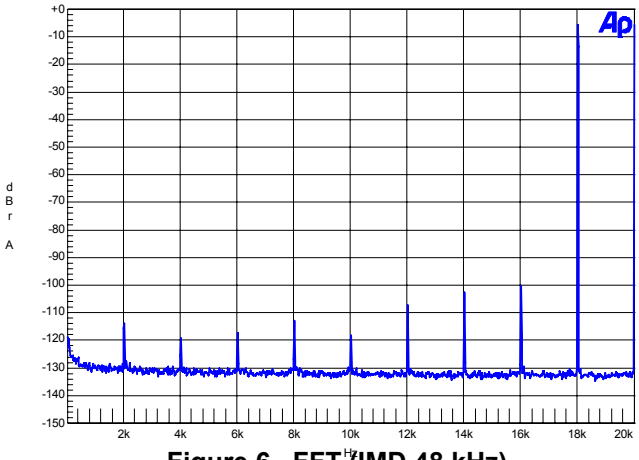



**Figure 6. FFT (IMD 48 kHz)**

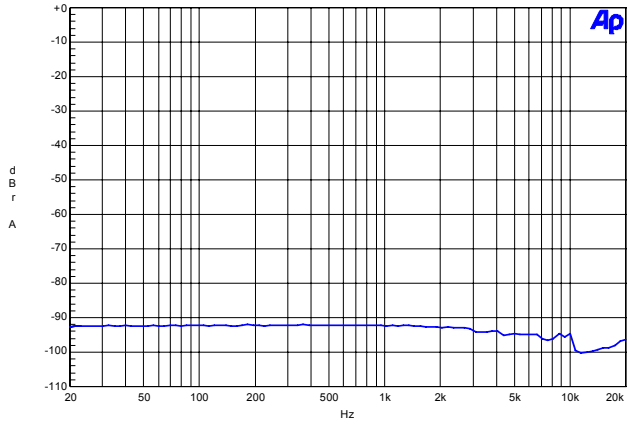



**Figure 7. 48 kHz THD+N vs. Input Freq**

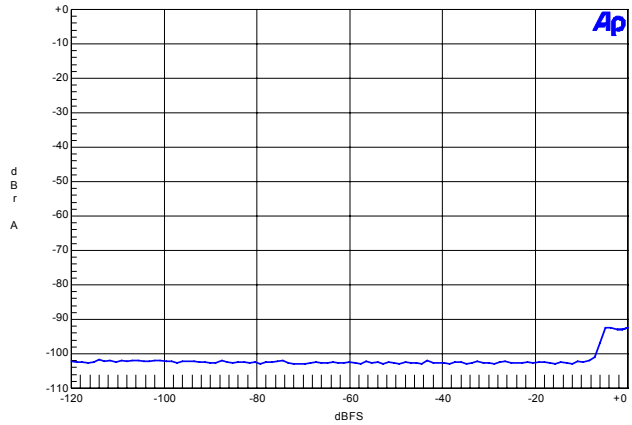



**Figure 8. 48 kHz THD+N vs. Level**

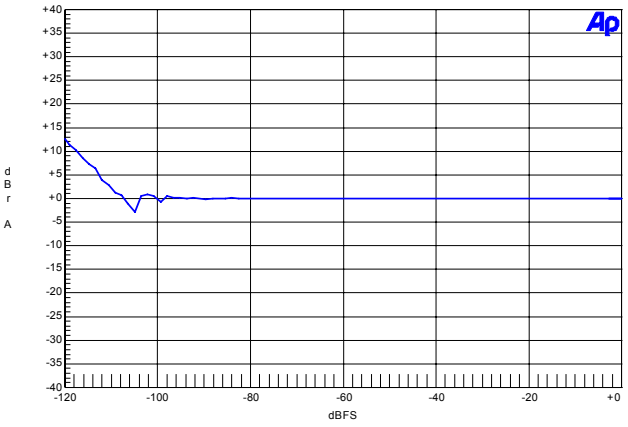



**Figure 9. 48 kHz, Fade-to-Noise Linearity**

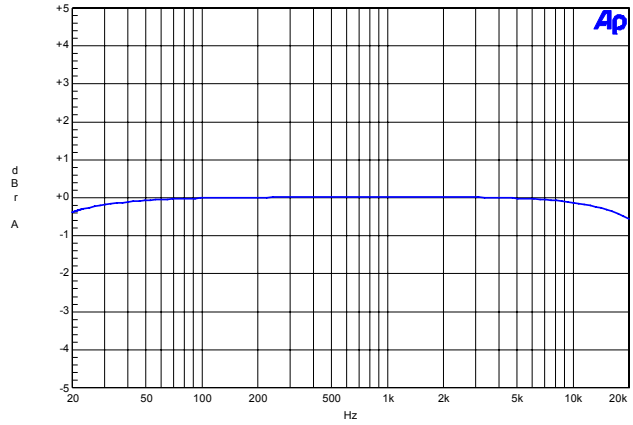



**Figure 10. 48 kHz, Frequency Response**

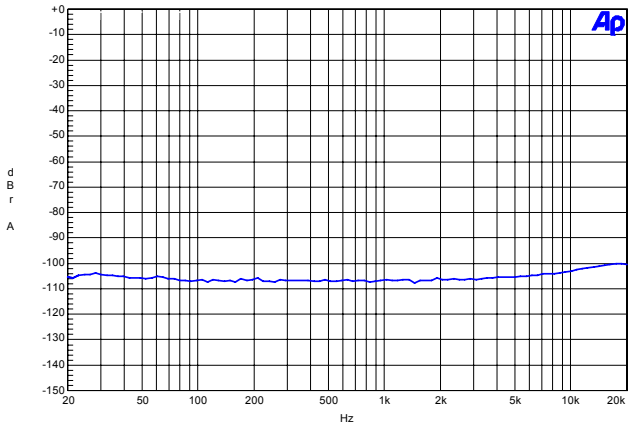



Figure 11. 48 kHz, Crosstalk

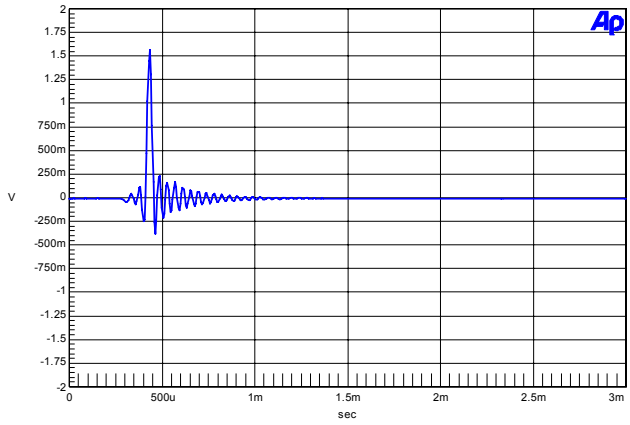



Figure 12. 48 kHz, Impulse Response

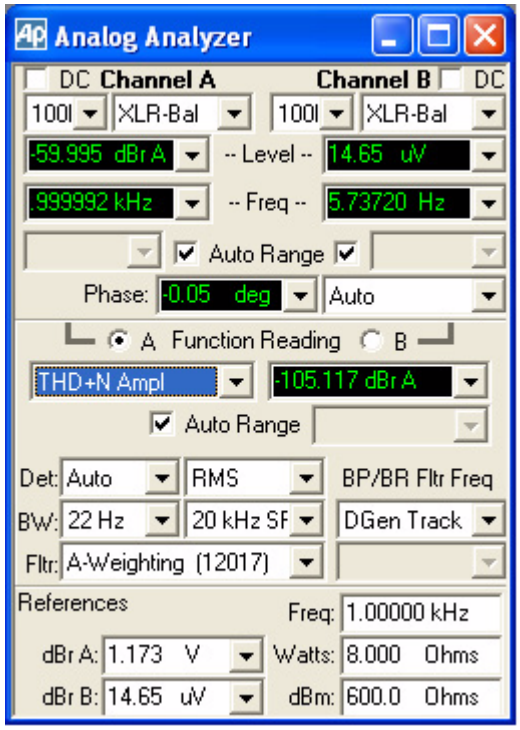



Figure 13. Dynamic Range 48 kHz

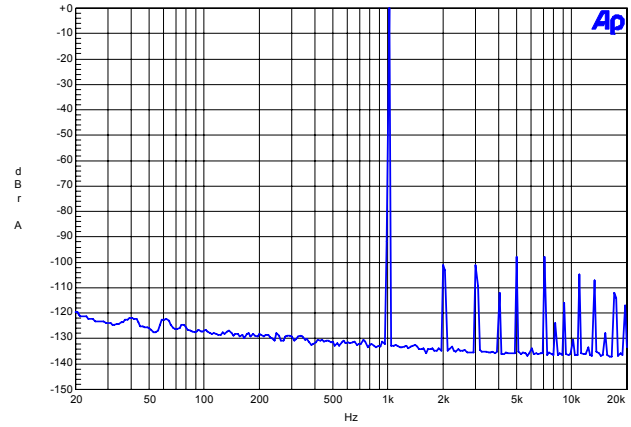



**Figure 14. FFT (96 kHz, 0 dB)**

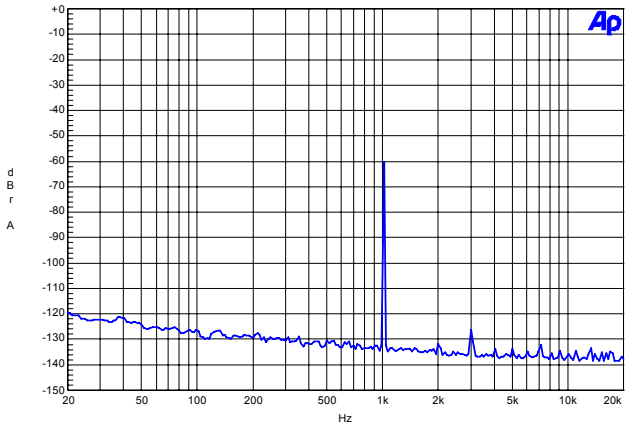



**Figure 15. FFT (96 kHz, -60 dB)**

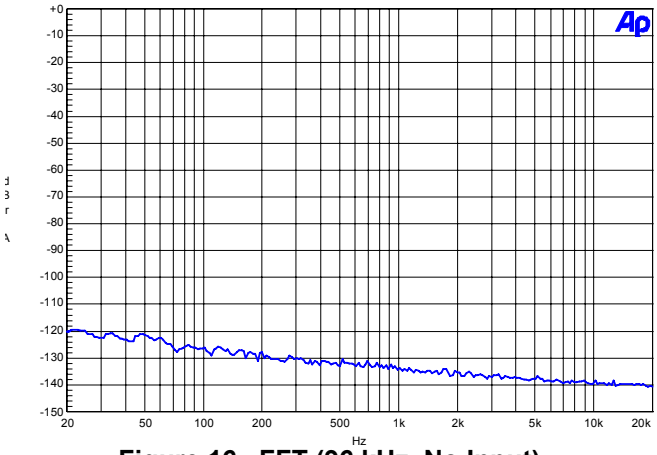



**Figure 16. FFT (96 kHz, No Input)**

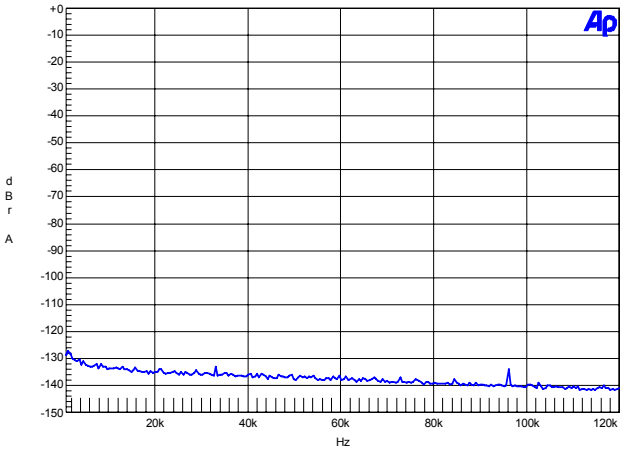



**Figure 17. FFT (96 kHz Out-of-Band, No Input)**

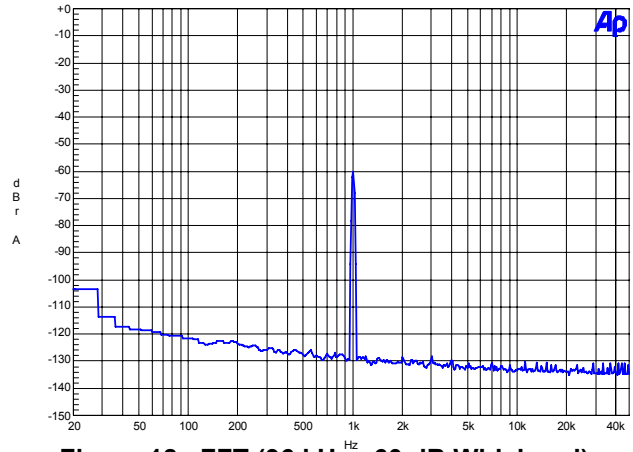



**Figure 18. FFT (96 kHz, -60 dB Wideband)**

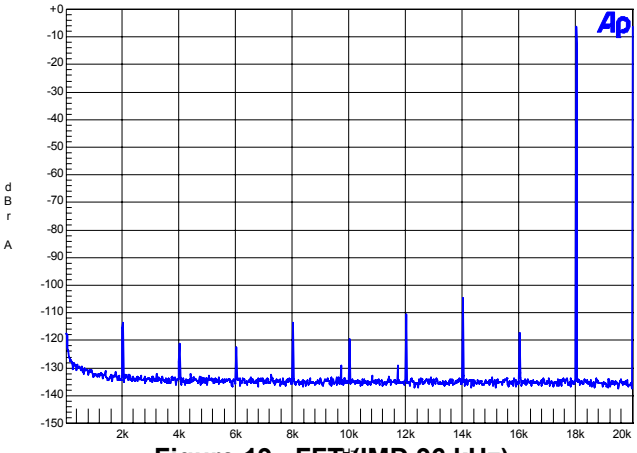



**Figure 19. FFT (IMD 96 kHz)**

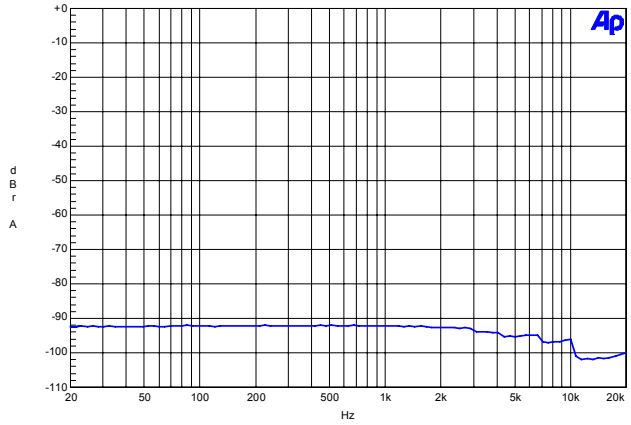



**Figure 20. 96 kHz, THD+N vs. Input Freq**

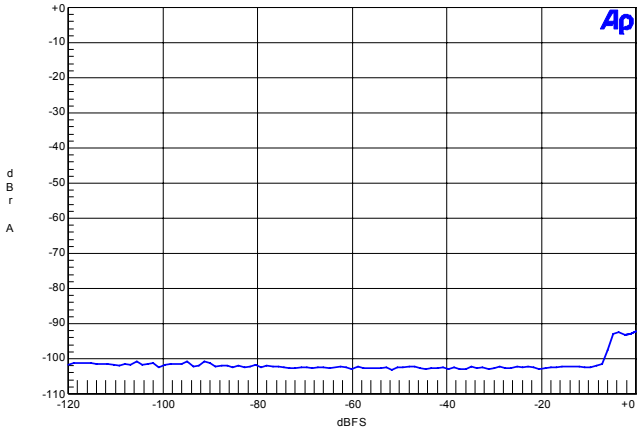



**Figure 21. 96 kHz, THD+N vs. Level**

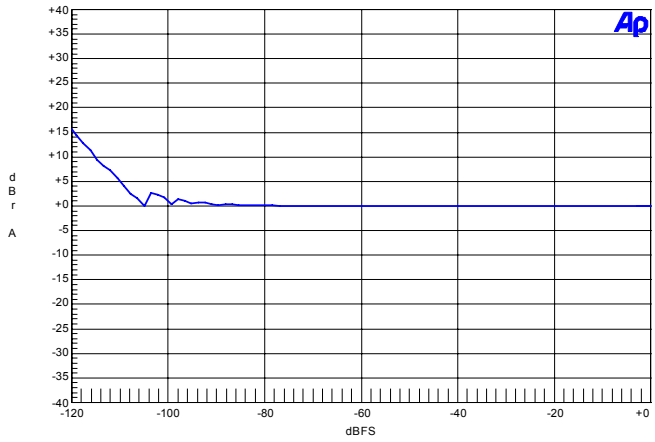



**Figure 22. 96 kHz, Fade-to-Noise Linearity**

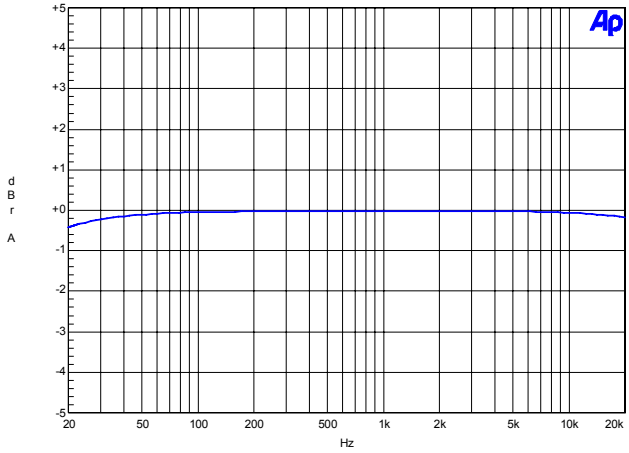



**Figure 23. 96 kHz, Frequency Response**

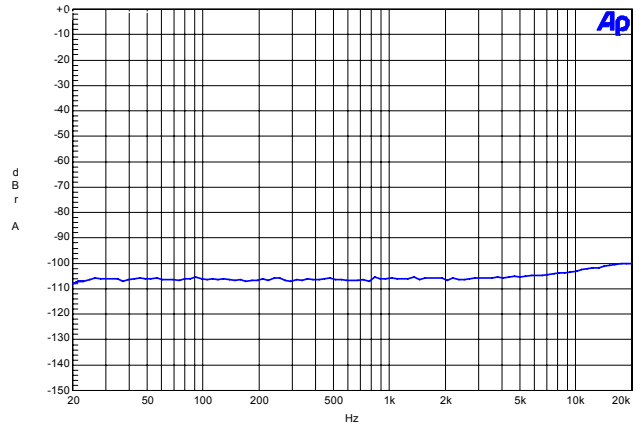



**Figure 24. 96 kHz, Crosstalk**

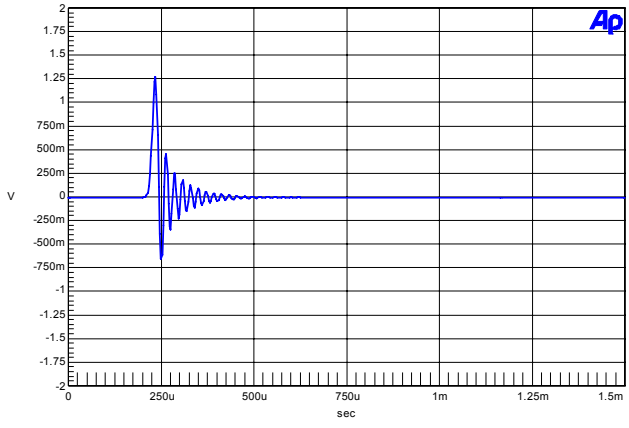



**Figure 25. 96 kHz, Impulse Response**

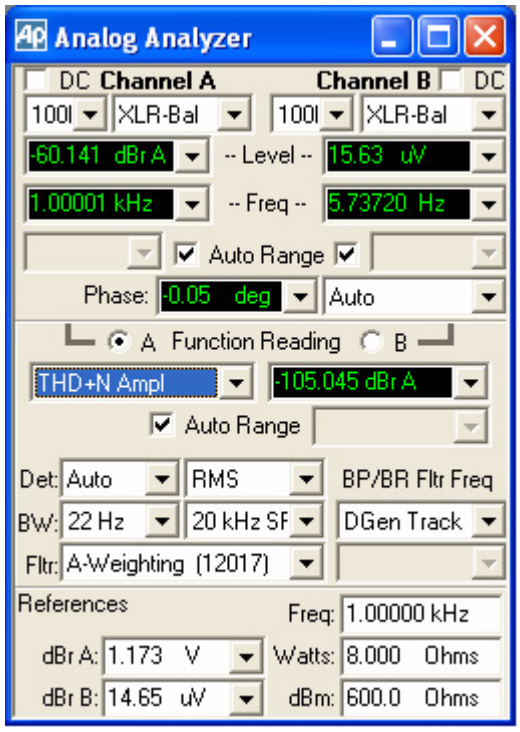



**Figure 26. Dynamic Range 96 kHz**

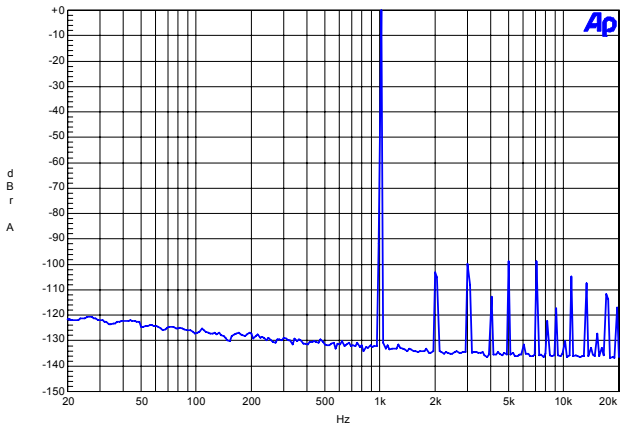



**Figure 27. FFT (192 kHz, 0 dB)**

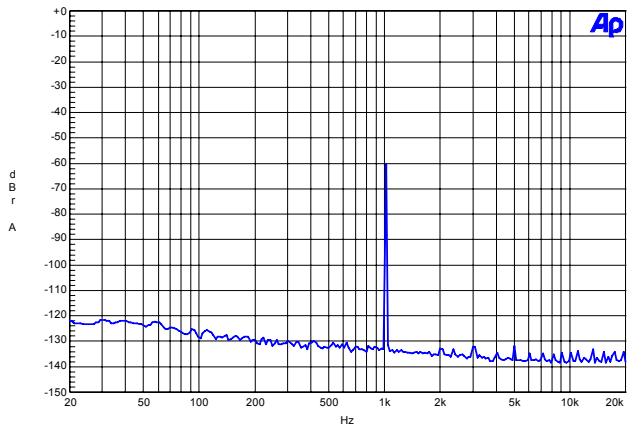



**Figure 28. FFT (192 kHz, -60 dB)**

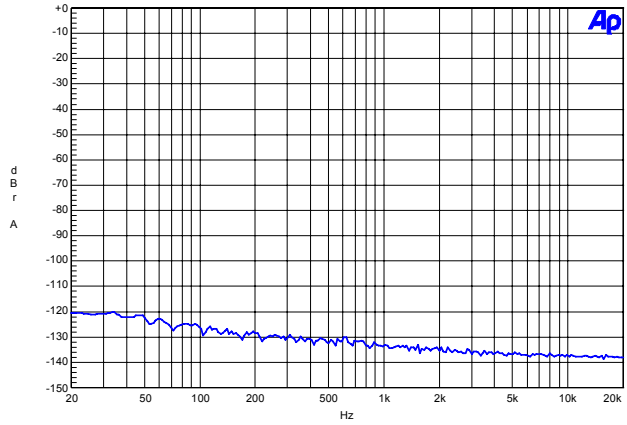



Figure 29. FFT (192 kHz, No Input)

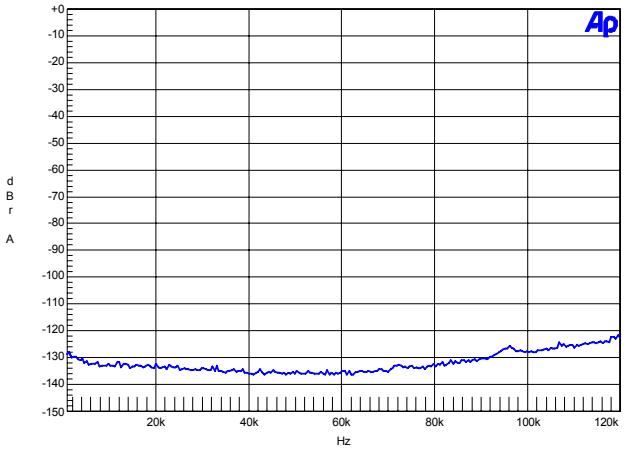



Figure 30. FFT (192 kHz Out-of-Band, No Input)

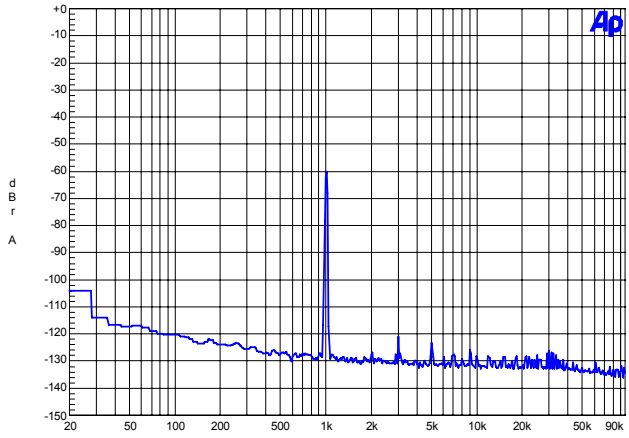



Figure 31. FFT (192 kHz, -60 dB Wideband)

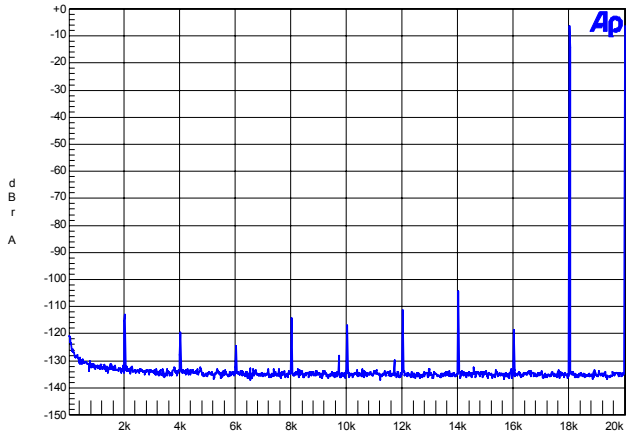



Figure 32. FFT (IMD 192 kHz)

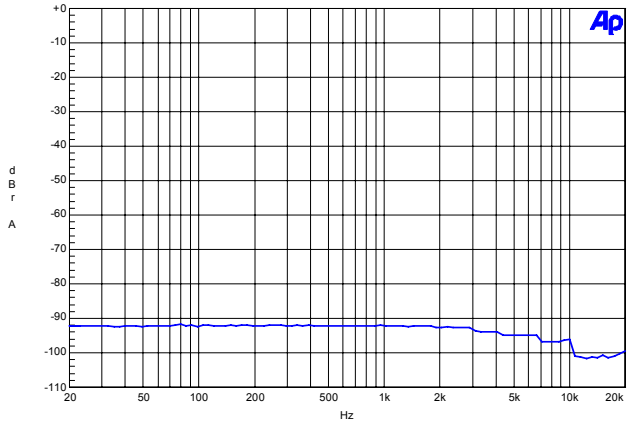



Figure 33. 192 kHz, THD+N vs. Input Freq

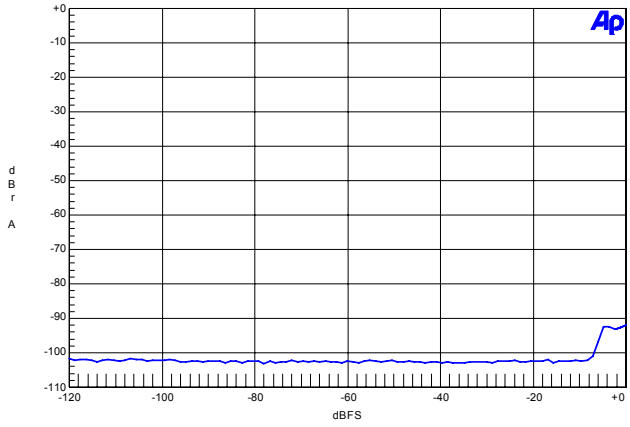



Figure 34. 192 kHz, THD+N vs. Level

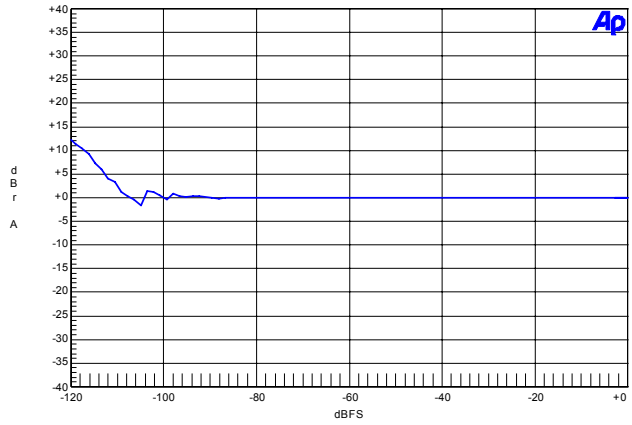



**Figure 35. 192 kHz, Fade-to-Noise Linearity**

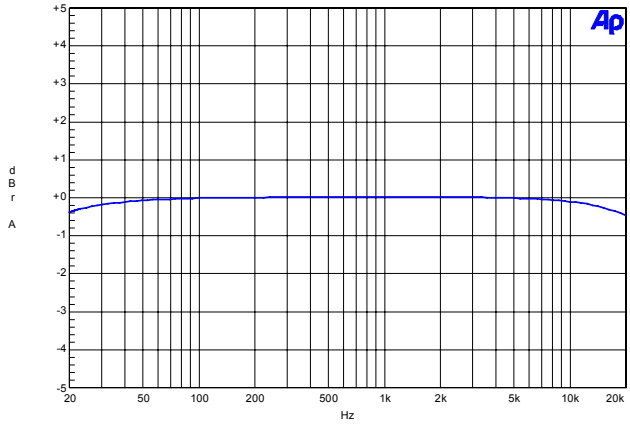



**Figure 36. 192 kHz, Frequency Response**

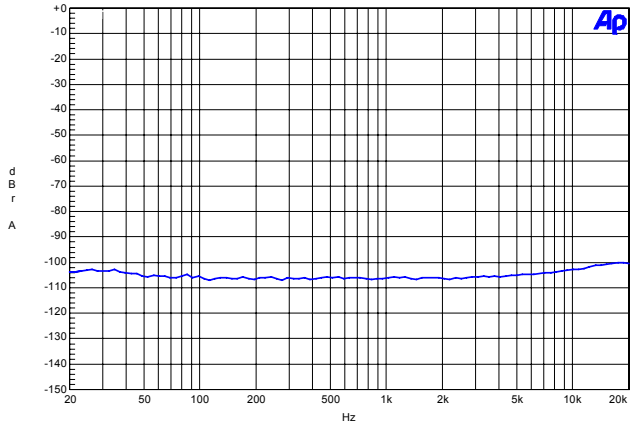



**Figure 37. 192 kHz, Crosstalk**

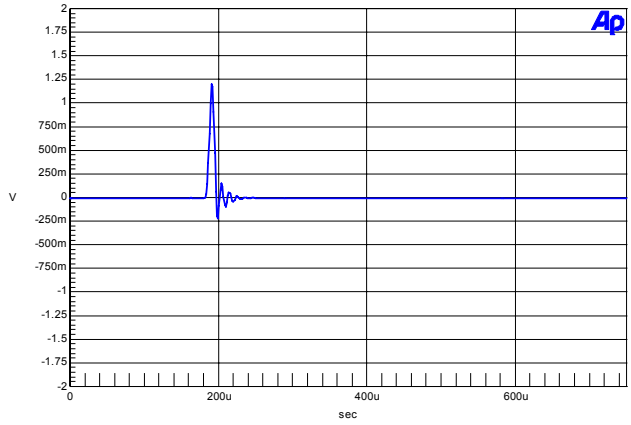



**Figure 38. 192 kHz, Impulse Response**

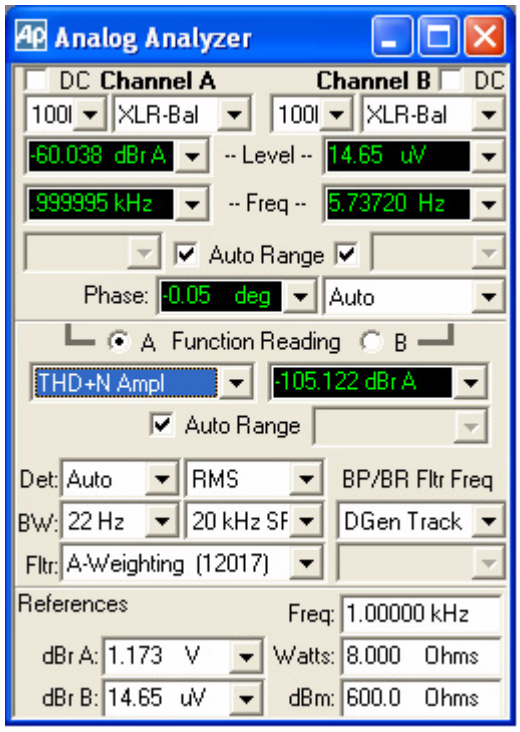



**Figure 39. Dynamic Range 192 kHz**

## 9. ERRATA

None at this time.

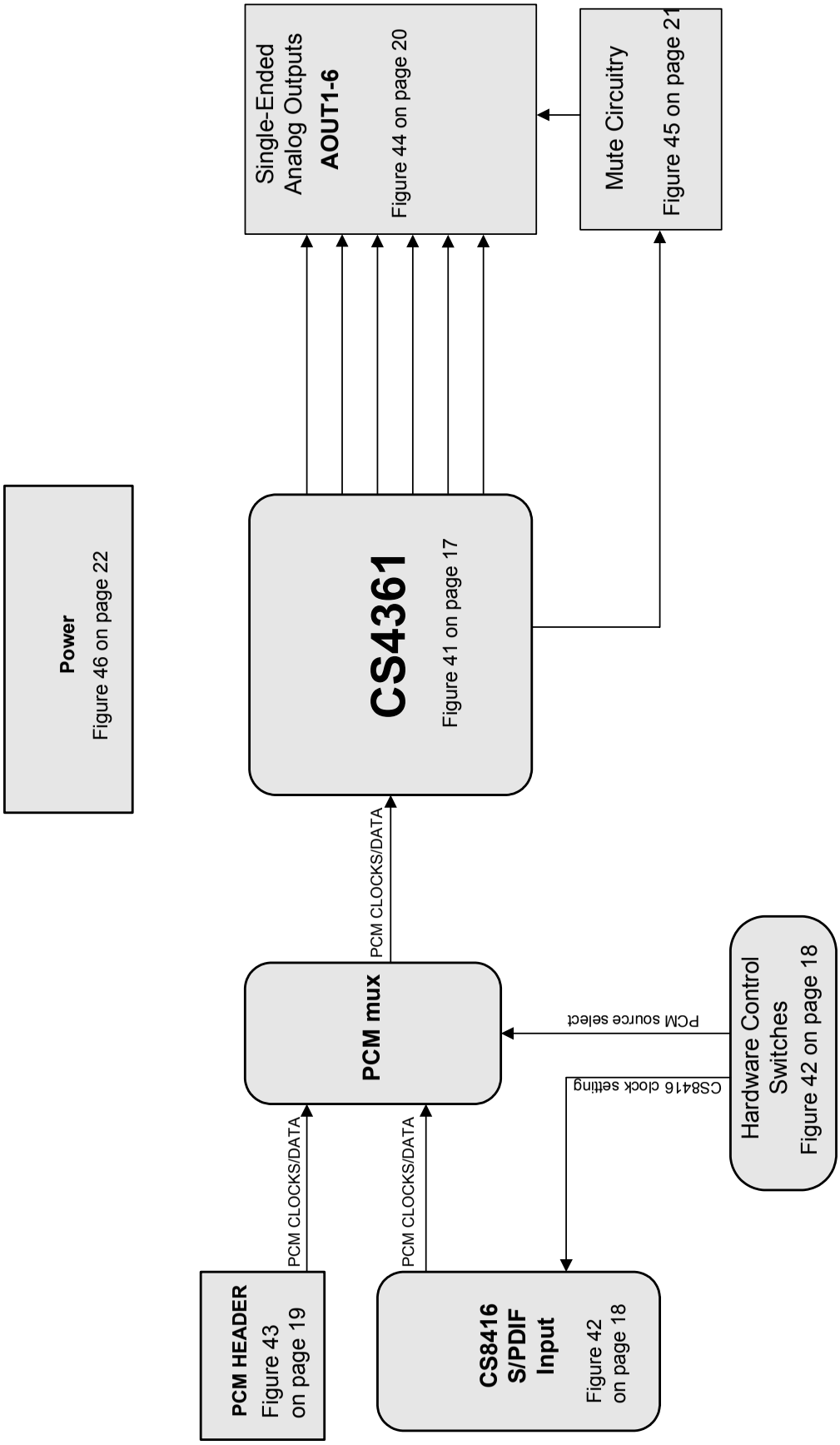



**Figure 40. System Block Diagram and Signal Flow**

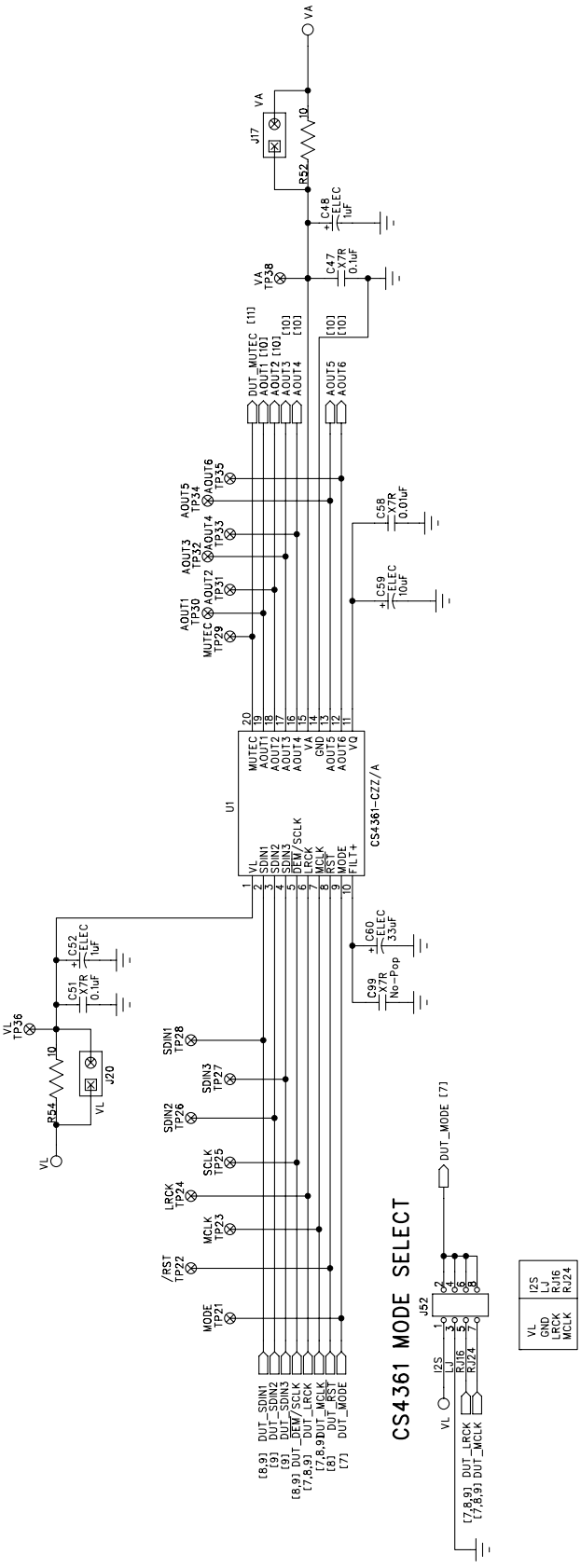
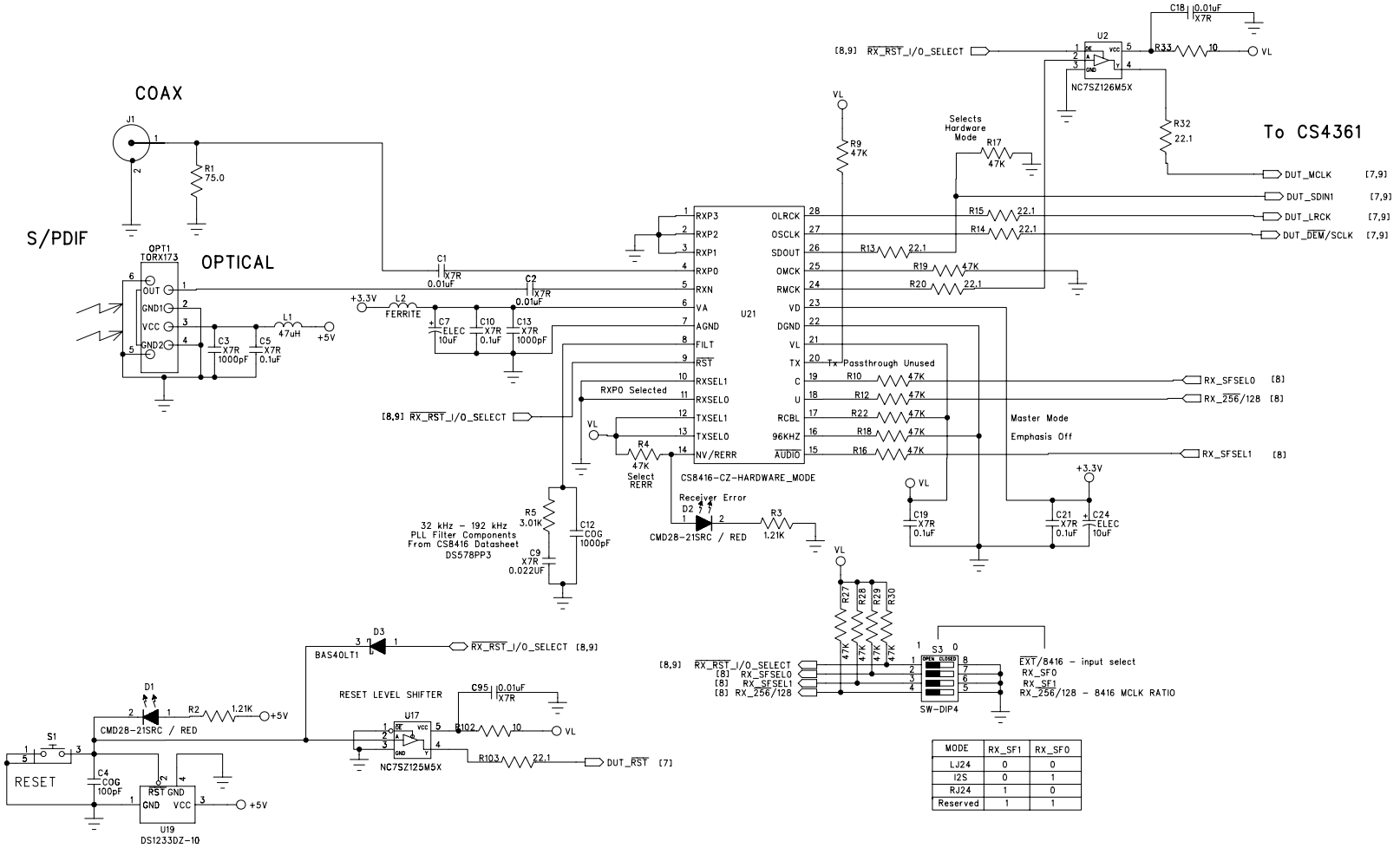



Figure 41. CS4361




| MODE | RX_SF1 | RX_SF0 |
|---|---|---|
| LJ24 | 0 | 0 |
| I2S | 0 | 1 |
| RJ24 | 1 | 0 |
| Reserved | 1 | 1 |

**Figure 42. CS8416 S/PDIF Input and Clock Control**

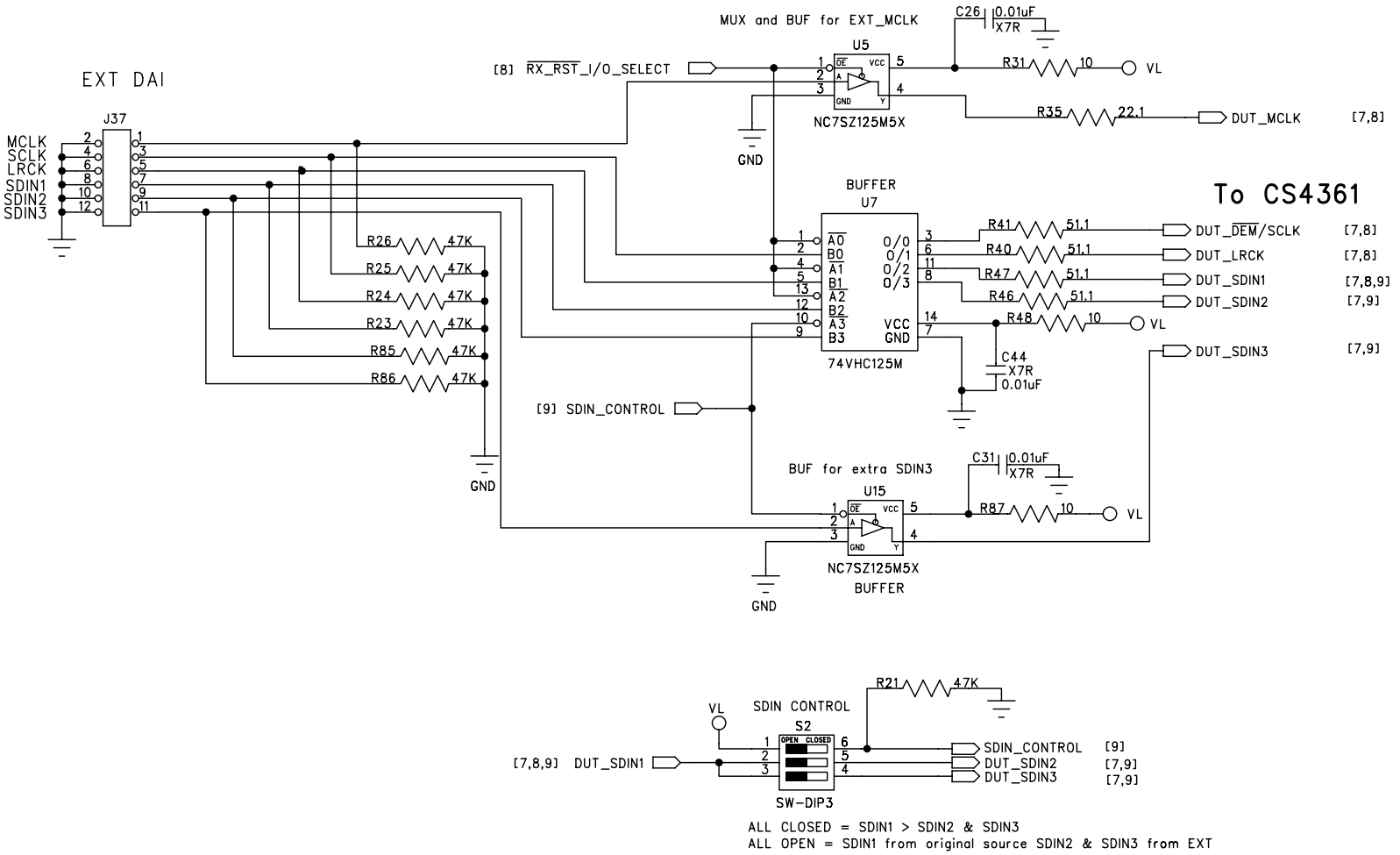



**Figure 43. PCM Input Header and MUX**

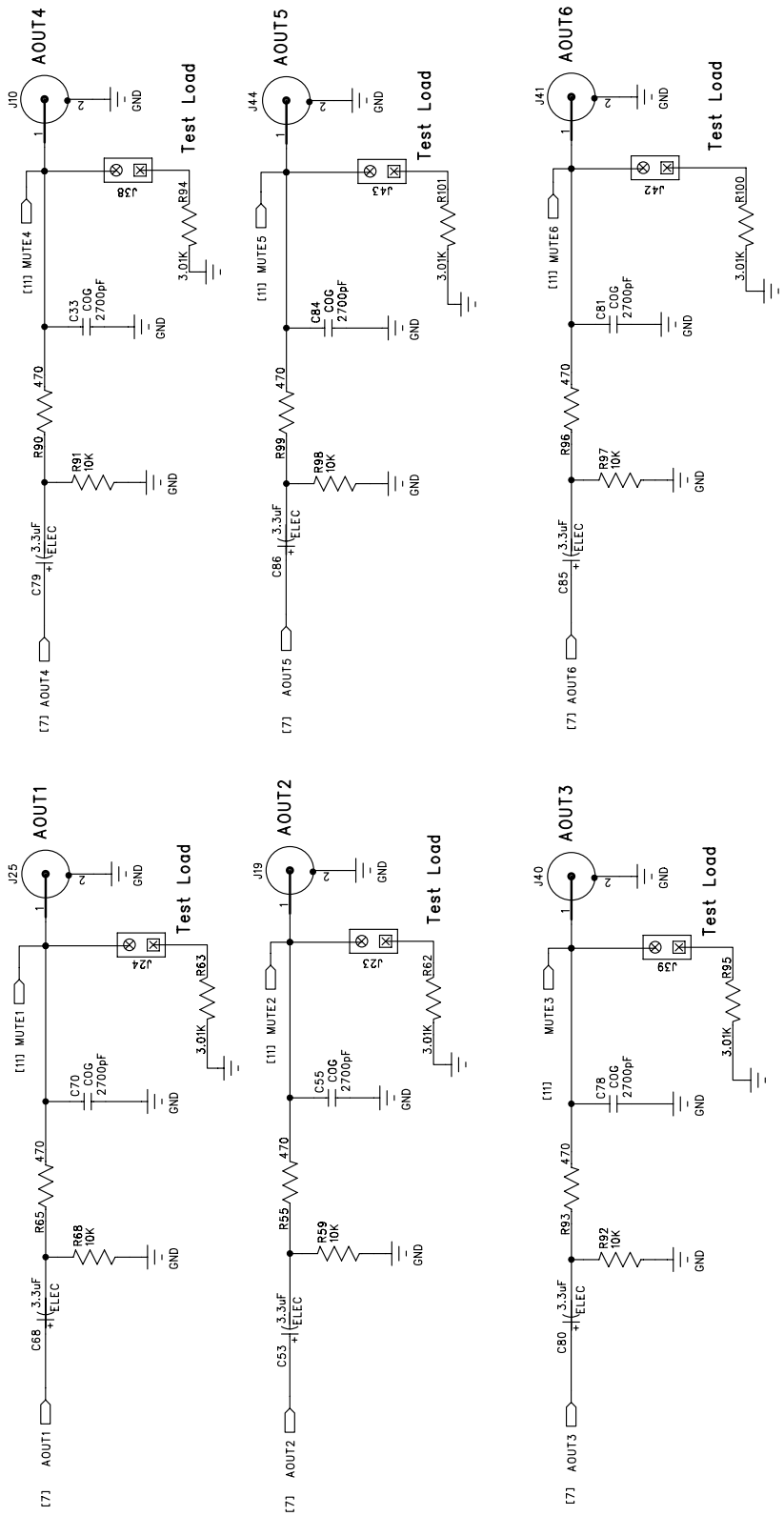



**Figure 44. Passive Outputs**

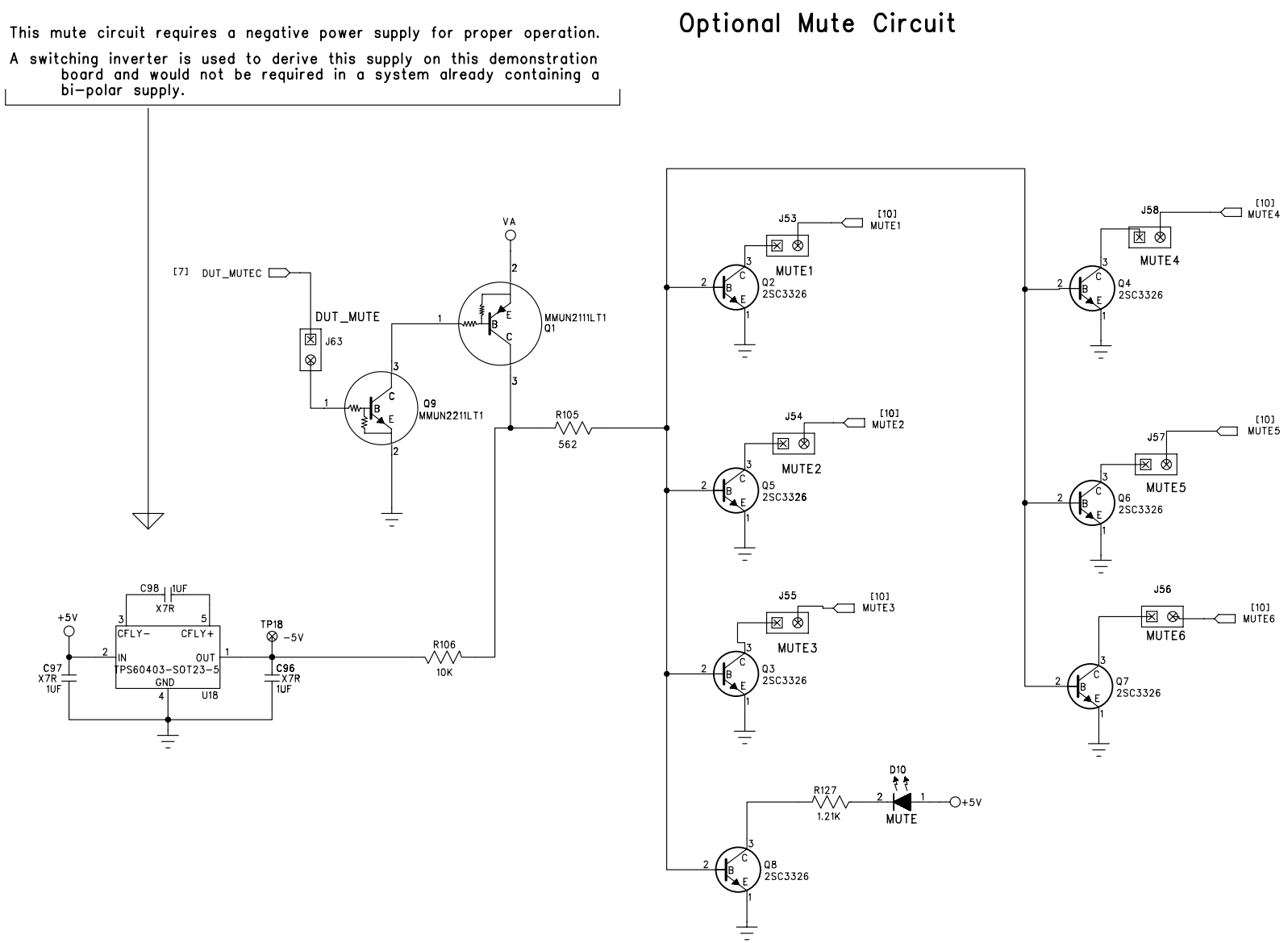



**Figure 45. Mute Circuitry**

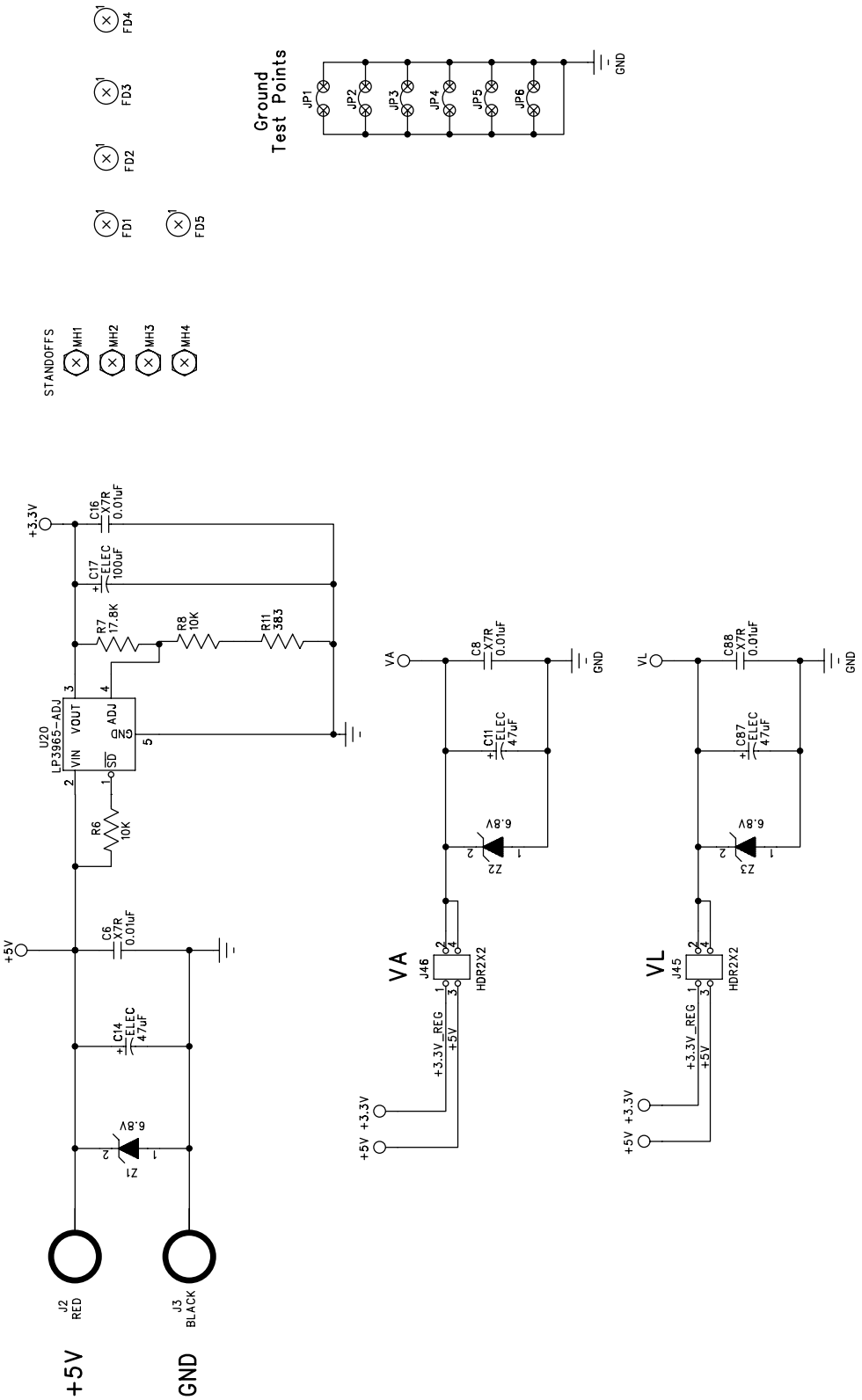



**Figure 46. Power Supply Connections**

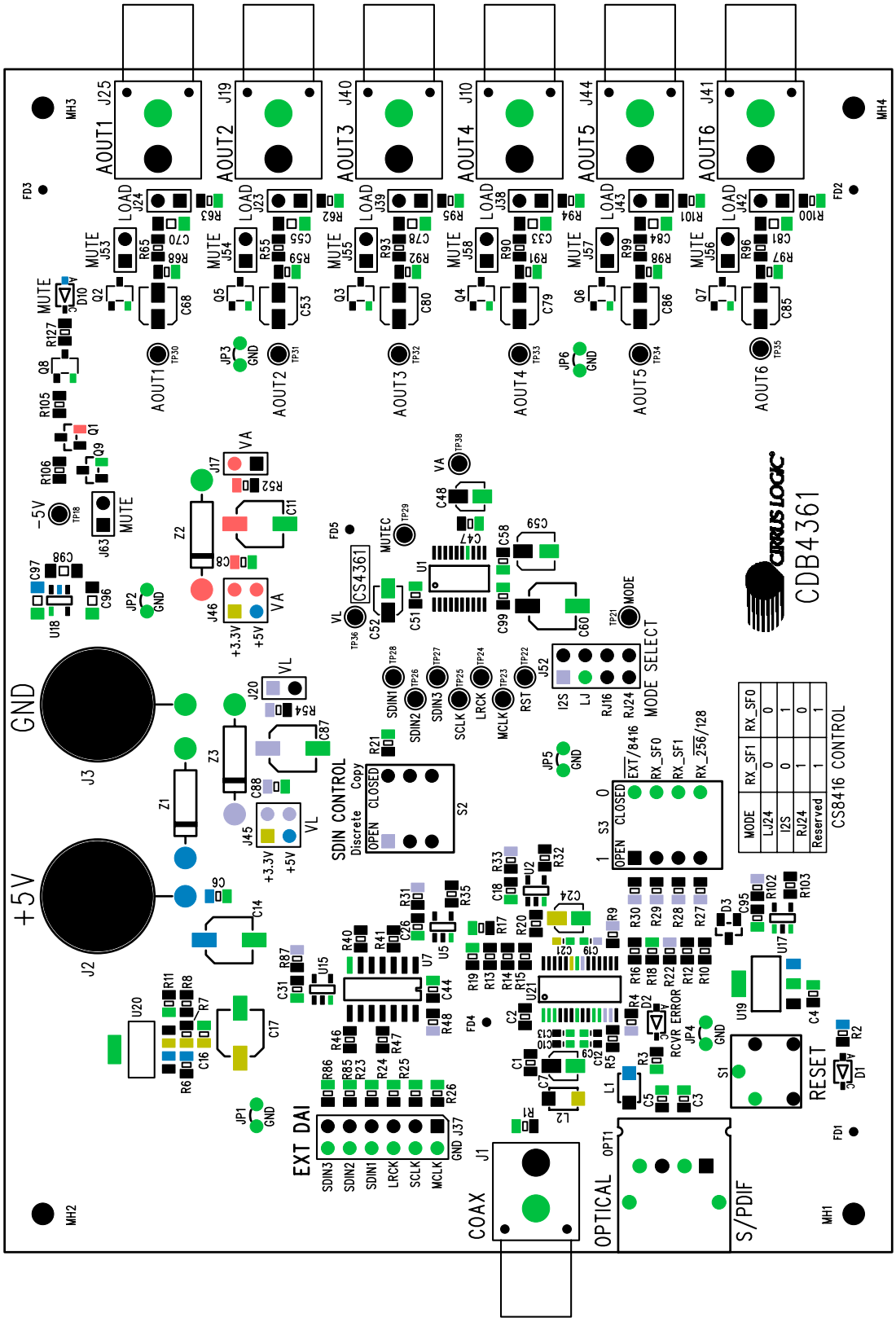



**Figure 47. Silkscreen Top**

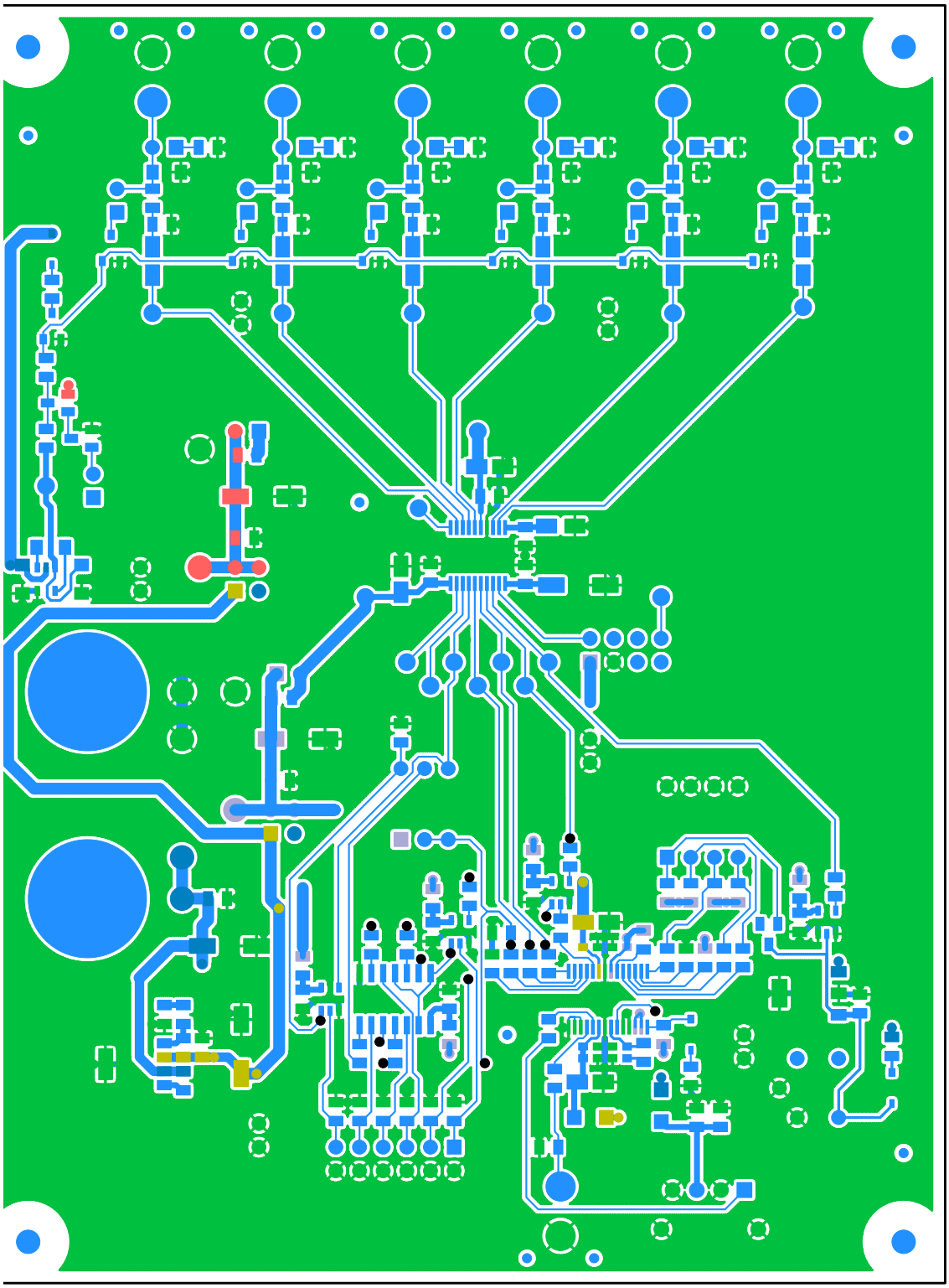



Figure 48. Top Side

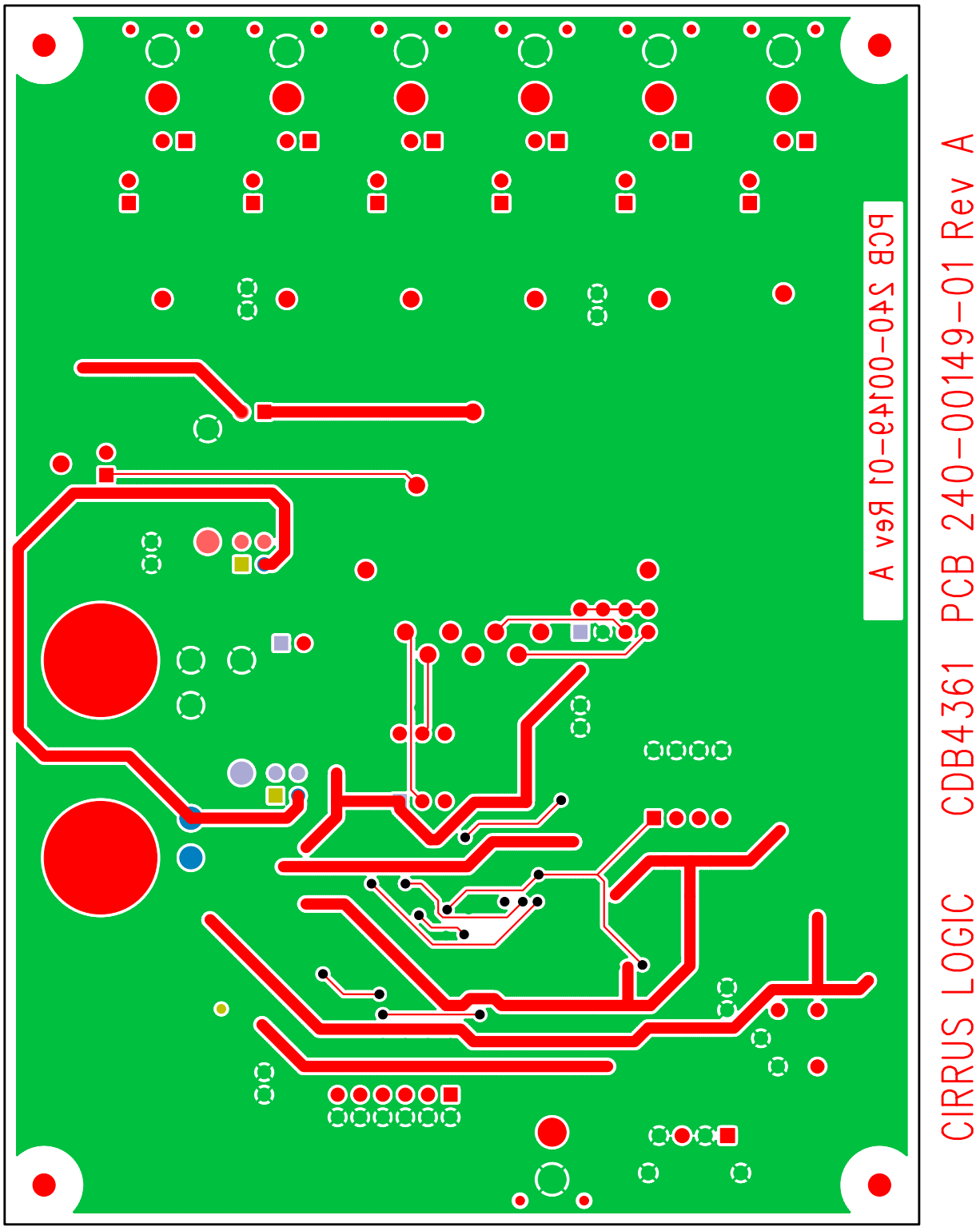



Figure 49. Bottom Side

# 10.REVISION HISTORY

| Release | Changes |
|---|---|
| DB1 | Initial Release |
| DB2 | Added Performance Plots |

## Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.

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